

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

LIBERTY PATENTS LLC,

Plaintiff,

v.

NXP SEMICONDUCTORS N.V., NXP
B.V., NXP USA, INC. D/B/A NXP
SEMICONDUCTORS USA, INC.,

Defendants.

CIVIL ACTION NO. 6:21-cv-693

ORIGINAL COMPLAINT FOR
PATENT INFRINGEMENT

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Liberty Patents LLC (“Liberty Patents” or “Plaintiff”) files this original complaint against Defendants NXP Semiconductors N.V., NXP B.V., and NXP USA, Inc. d/b/a NXP Semiconductors USA, Inc., (collectively “NXP” or “Defendants”), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

PARTIES

1. Liberty Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas, 75703.

2. Defendant NXP Semiconductors N.V. is a company organized and existing under the laws of The Netherlands. NXP Semiconductors N.V. has an office at High Tech Campus 60, 5656 AG Eindhoven, The Netherlands. NXP Semiconductors N.V. may also be served with process by serving the Texas Secretary of State, 1019 Brazos Street, Austin, Texas, 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a

resident agent for service of process in Texas as required by statute. This action arises out of that business.

3. Defendant NXP B.V. is a company organized and existing under the laws of The Netherlands. NXP B.V. has an office at High Tech Campus 60, 5656 AG Eindhoven, The Netherlands. NXP B.V. may also be served with process by serving the Texas Secretary of State, 1019 Brazos Street, Austin, Texas, 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a resident agent for service of process in Texas as required by statute. This action arises out of that business.

4. NXP B.V. is a wholly owned subsidiary of NXP Semiconductors N.V. NXP B.V. develops and sells semiconductor devices globally. Its corporate parent, NXP Semiconductors N.V., does business globally through NXP B.V and NXP B.V.’s subsidiary companies.

5. Defendant NXP USA, Inc. d/b/a NXP Semiconductors USA, Inc. (“NXP USA”) is a corporation organized and existing under the laws of Delaware. NXP USA may be served with process through its registered agent, Corporation Service Company d/b/a/ CSC-Lawyers Incorporating Service Company at 211 East 7th Street, Suite 620, Austin, Texas, 78701-3218.

6. NXP USA is a subsidiary of both NXP Semiconductors N.V. and NXP B.V. According to its website, NXP operates three wafer fabrication facilities in the US through NXP USA—two of which are in Austin, Texas. These facilities manufacture “microcontrollers (MCUs) and microprocessors (MPUs), power management devices, RF transceivers, amplifiers and sensors.”¹

7. The Defendants identified in paragraphs 2 through 6 above are companies which together comprise “a global semiconductor company and a long-standing supplier in the

¹ See www.nxp.com/company/about-nxp/worldwide-locations/united-states:USA.

industry, with over 50 years of innovation and operating history.”² According to NXP, it provides technology solutions in the fields of cryptography-security, high-speed interface, radio frequency (RF), mixed-signal analog-digital (mixed A/D), power management, digital signal processing and embedded system design. Its products are used in a wide range of end-market applications, including automotive, industrial & Internet of Things (IoT), mobile, and communication infrastructure.³

8. The NXP Defendants named above and their affiliates are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular. For example, NXP explains that the commercial name for NXP group of companies is “NXP” or “NXP Semiconductors.”⁴

9. The NXP Defendants named above and their affiliates share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and accused product lines and products involving related technologies.

10. Thus, the NXP Defendants named above and their affiliates operate as a unitary business venture and are jointly and severally liable for the acts of patent infringement alleged herein.

² See NXP Semiconductors N.V.’s Form 10-K Annual Report, at 3 (Feb. 27, 2020), <https://investors.nxp.com/sec-filings/sec-filing/10-k/0001413447-20-000009>.

³ *Id.*

⁴ *Id.*

JURISDICTION AND VENUE

11. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

12. This Court has personal jurisdiction over the NXP Defendants pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) NXP has done and continues to do business in Texas; (ii) NXP has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing at least a portion of any other infringements alleged herein in Texas, and (iii) NXP regularly places its products within the stream of commerce—directly, through subsidiaries, or through third parties—with the expectation and knowledge that such products will be shipped to, sold, or used in Texas and elsewhere in the United States. Thus, the NXP Defendants have established minimum contacts within Texas and purposefully availed themselves of the benefits of Texas, and the exercise of personal jurisdiction over the NXP Defendants would not offend traditional notions of fair play and substantial justice. In addition, or in the alternative, this Court has personal jurisdiction over NXP Semiconductors N.V. and NXP B.V. pursuant to Federal Rule of Civil Procedure 4(k)(2).

13. Venue is proper in this district under 28 U.S.C. § 1400(b) because (i) NXP has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a

portion of any other infringements alleged herein in this district, (ii) NXP Semiconductors N.V. and NXP B.V. are foreign entities, (iii) NXP USA is registered to do business in Texas, and (iv) NXP USA has regular and established places of business in this district, including at least at 6501 W. William Cannon Drive, Austin, Texas, 78735, and at 3501 Ed Bluestein Blvd., Austin, Texas, 78721:

NXP Locations in the United States

Austin, TX (ATMC) Manufacturing 3501 Ed Bluestein Blvd., Austin, TX 78721 Directions	Chandler, AZ Design, Manufacturing 1300 North Alma School Rd Chandler, AZ 85224 Directions	Hoffman Estates, IL Sales 2800 West Higgins Rd., Suite 600 Hoffman Estates, IL 60169 (847) 843-6810 Directions	Irvine, CA Sales 6410 Oak Canyon, Suite 200 Irvine, CA 92618 Directions
Austin, TX (Oak Hill) US Corporate Headquarters, Design, Manufacturing 6501 W. William Cannon Dr. Austin, TX 78735 Directions	Kokomo, IN Sales 2733 South Albright Rd, Kokomo, IN 46902 Directions	Novi, MI Design, Sales Haggerty Corp. Office Center V 28125 Cabot Dr. Suite 100, Novi, MI 48377 Directions	San Diego, CA Sales Innovation Drive, Suite 150, San Diego, CA 92128 Directions

Source: www.nxp.com/company/about-nxp/worldwide-locations/united-states:USA

BACKGROUND

14. The patents-in-suit generally relate to body biasing voltages used in integrated circuits (ICs). They teach application of body biasing techniques that improve circuit performance and reduce power consumption in one or more power modes. Specifically, the patents-in-suit disclose systems and methods for generating body biasing voltages so that a processor can operate with increased power savings. For example, the patents-in-suit describe techniques for using body biasing voltages to decrease power consumption during high performance applications. Other examples disclose use of body biasing voltages during low-power modes.

15. The use of body biasing voltages in ICs has become an increasingly necessary design feature in many applications today. Coupled with the explosive demand for ICs over the last few years, the more stringent requirement that ICs consume less and less power has focused the industry towards using body biasing voltages. Body biasing voltage techniques are now being used in applications ranging from automotive technologies to industrial IoT devices. Whether an application requires high performance circuitry or ultra low-power modes (or both), body biasing techniques have become essential.

16. The technology described by the patents-in-suit was developed by engineers at Transmeta Corp. Transmeta was a technology company formed in 1995 and best known for designing high performance processors, such as the Crusoe and the Efficeon in the early 2000s. In particular, Transmeta's major focus was on developing low power, high performance ICs. To achieve such high power savings, one of the major techniques used by Transmeta engineers was to apply body biasing voltages to its ICs.

17. Industry experts have recognized the technological innovation of Transmeta's processors, and some have noted that Transmeta's energy-saving processors were ahead of their time.⁵ The inventions disclosed in the patents-in-suit are extremely important to multiple industries, and have been cited by major technology companies and processor developers like Canon, Freescale Semiconductor (now part of NXP), Nvidia, Packet Digital, and Smart Technologies (now part of Foxconn).

⁵ See, e.g., *Chip Hall of Fame: Transmeta Corp. Crusoe Processor*, IEEE Spectrum (June 30, 2017) (“Ahead of its time, this chip heralded the mobile era when energy use, not processing power, would become the most important spec.”), <https://spectrum.ieee.org/tech-history/silicon-revolution/chip-hall-of-fame-transmeta-corp-crusoe-processor>.

COUNT I

DIRECT INFRINGEMENT OF U.S. PATENT NO. 7,509,504

18. On March 24, 2009, U.S. Patent No. 7,509,504 (“the ’504 Patent”) was duly and legally issued by the United States Patent and Trademark Office for an invention entitled “Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems.”

19. Liberty Patents is the owner of the ’504 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the ’504 Patent against infringers, and to collect damages for all relevant times.

20. NXP made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, NXP’s i.MX 7ULP Applications Processor and other products⁶ that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit (“accused products”):



i.MX 7ULP Family: Ultra-Low-Power with Graphics

Source: www.mouser.com/new/nxp-semiconductors/nxp-imx-7ulp-applications-processors/;
www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-7-processors/i-mx-7ulp-family-ultra-low-power-with-graphics:i.MX7ULP

⁶ See, e.g., NXP’s MCIMX7U5DVP07SC, MCIMX7U5DVK07SC, MCIMX7U3DVK07SC, MCIMX7U5CVP06SC, MCIMX7U3CVP06SC, MCIMX7U5DVP08SC, MCIMX7U3CVP06SD, MCIMX7U5CVP06SD, MCIMX7ULP-EVK, etc.

21. By doing so, NXP has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '504 Patent. NXP's infringement in this regard is ongoing.

22. NXP's i.MX 7ULP Applications Processor is an exemplary accused product.

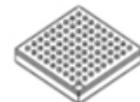
23. NXP has infringed the '504 Patent by using the accused products and thereby practicing a method for determining a body biasing voltage applied to a microprocessor.

24. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP's processors support different body biasing voltages for different power modes. Accordingly, the i.MX 7ULP Applications Processor practices a method for determining a body biasing voltage that is to be applied to the processor.

i.MX 7ULP Applications Processor—Consumer Products

The i.MX 7ULP product family members are optimized for power-sensitive applications benefiting from NXP's Heterogeneous Multicore Processing (HMP) architecture. Achieving an efficient balance between processing power and deterministic processing needs, the i.MX 7ULP is an asymmetric processor consisting of two separate processing domains: an application domain and a real-time domain. The application domain is built around an ARM® Cortex®-A7 processor with an ARM NEON™ SIMD engine and floating point unit (FPU) and is optimized for rich OS based applications. The real-time domain is built around an ARM Cortex-M4 processor (with FPU) optimized for lowest possible leakage. Both domains are completely independent, with separate power, clocking, and peripheral domains, but the bus fabric of each domain is tightly integrated for efficient communication. The part is streamlined to minimize pin count, enabling small packages and simple system integration.

MCIMX7U5DVP07SC
MCIMX7U5DVK07SC
MCIMX7U3DVK07SC



Plastic packages: BGA 14x14mm, 0.5mm pitch, and BGA 10 x 10 mm, 0.5 mm pitch

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 1)

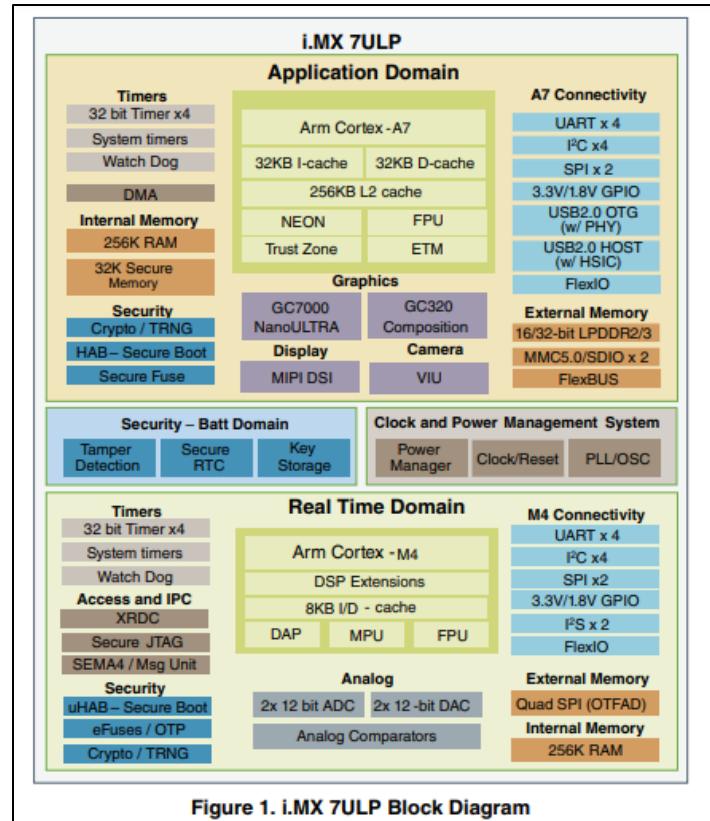


Figure 1. i.MX 7ULP Block Diagram

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 3)

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biasing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), VLPS and LLS modes

1. All options for FBB/RBB are fully programmable

i.MX 7ULP Applications Processor Reference Manual, Rev. 0, 06/2019

NXP Semiconductors

1149

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

25. The method practiced using the accused products comprises receiving a command to change to a different power condition of a computer system comprising the microprocessor.

The power condition comprises a different microprocessor clock frequency and/or a different microprocessor operating voltage.

26. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP's processors support multiple power modes, including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. The system provides a Multicore System Mode Control (MSMC) module for controlling and changing the power modes of both processors. The MSMC module works with the Power Management Controller (PMC) of each processor. The PMC allows user software to control and change the power modes of the processor—that is, the PMC of each processor can receive a command to change from HSRUN to VLPS (“said different power condition”), for example.

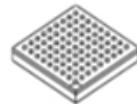
27. Power consumption is optimized in each power mode by changing the clock frequency and voltage. Accordingly, each of the different power modes, such as VLPS (“said different power condition”), of each processor is associated with a different clock frequency and a different voltage.

i.MX 7ULP Applications

Processor—Consumer Products

The i.MX 7ULP product family members are optimized for power-sensitive applications benefiting from NXP's Heterogeneous Multicore Processing (HMP) architecture. Achieving an efficient balance between processing power and deterministic processing needs, the i.MX 7ULP is an asymmetric processor consisting of two separate processing domains: an application domain and a real-time domain. The application domain is built around an ARM® Cortex®-A7 processor with an ARM NEON™ SIMD engine and floating point unit (FPU) and is optimized for rich OS based applications. The real-time domain is built around an ARM Cortex-M4 processor (with FPU) optimized for lowest possible leakage. Both domains are completely independent, with separate power, clocking, and peripheral domains, but the bus fabric of each domain is tightly integrated for efficient communication. The part is streamlined to minimize pin count, enabling small packages and simple system integration.

MCIMX7U5DVP07SC
MCIMX7U5DVK07SC
MCIMX7U3DVK07SC



Plastic packages: BGA 14x14mm, 0.5mm pitch, and BGA 10 x 10 mm, 0.5 mm pitch

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 1)

The following table describes the power modes available to each core within the MCU.

Table 30-5. Power modes

Mode	Description
Run (RUN)	The core can be run at full frequency and all functionality is available. This mode is also referred to as Normal Run mode.
High Speed Run (HSRUN)	Provides the highest performance mode at the fastest supported frequency. The core, system, bus, and flash clock maximum frequencies are unrestricted in this mode. ¹
Wait (WAIT)	Allows a core to enter a static, low power state with instant wakeup time, while still allowing peripherals to operate with full functionality. The core clock is gated off. The system clock continues to operate. Bus clocks, if enabled, continue to operate.
Stop (STOP)	Allows a core and its peripherals to enter a static, low power state with relatively fast wakeup times, while still allowing peripherals to operate with full asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Very Low Power Run (VLPR)	Provides the lowest power operating mode to the core at a reduced frequency. The core, system, bus, and flash clock maximum frequencies are restricted in this mode. ¹
Very Low Power Wait (VLPW)	Allows a core to enter a static, very low power state, while still allowing peripherals to operate with full functionality at a reduced frequency. The core clock is gated off. The system, bus, and flash clocks continue to operate, although their maximum frequency is restricted. ¹
Very Low Power Stop (VLPS)	Allows a core and its peripherals to enter a static, very low power state with relatively fast wakeup times, while still allowing peripherals to operate with limited asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Low Leakage Stop (LLS)	Allows a core and its peripherals to enter a low leakage, power gated state with relatively fast wakeup times, while still retaining the state of all logic. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic and I/O are retained, with wakeup only supported via the LLWU, NMI or Reset pins.
Very Low Leakage Stop (VLLS)	Allows a core and its peripherals to enter a very low leakage, power gated state. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic is power gated, with wakeup only supported via the LLWU, NMI or Reset pins. I/O states are latched.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1242)

27.11 Power modes

27.11.1 A7 domain power

The A7 domain has multiple power modes. The following table describes the state of A7 domain in those modes.

Table 27-5. A7 power modes

A7 Power Mode	Description	Recovery Method	Recovery Time
<u>HSRUN</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • Allows FBB (optional) • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
<u>RUN</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • FBB/RBB not allowed. • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
<u>VLPR</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Max Frequency restricted to FIRC (48 MHz). PLLs disabled. • Option to disable LVD/HVD 	N/A	N/A

Table continues on the next page...

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1153)

Power modes			
Table 27-5. A7 power modes (continued)			
A7 Power Mode	Description	Recovery Method	Recovery Time
	<ul style="list-style-type: none"> DDR in self-refresh mode. DDR self-refresh must be done by software by writing to MMDC_MAPSR[LPMD] bit RBB not allowed 		
WAIT ^{1, 2}	<ul style="list-style-type: none"> Allows Peripherals to function while keeping core in sleep (clock-gated). A7 processor in Wait-for-Interrupt (WFI) state. 	Interrupt ³ /Reset ⁴	0 ns
STOP ⁵ /VLPS	<ul style="list-style-type: none"> IMX 7ULP is in static state with all registers retained with maintaining LVD protection. RBB only allowed in VLPS mode. FIRCCSR[FIRCLPEN] in the SCG module, keeps FIRC enabled in VLPS mode. LVDs could be turned off in VLPS mode. 	Interrupt/Reset ⁴	7 µs(STOP) and 23 µs (VLPS with RBB)/21.5 µs (VLPS without RBB) ⁶
LLS ⁷	<ul style="list-style-type: none"> A7 supply ON RBB is allowed LVD protection IO supplies ON A7 processor is in a wait-for-interrupt (WFI) state. The core clock is gated. Bus and DMA clocks are gated All peripheral clocks are gated. SRAM contents are retained. DDR can be in self-refresh 	Interrupt/Reset ⁴	Wake up time: 41.5 µs (LLS with RBB)/40 µs (LLS without RBB) ⁸
VLLS	<ul style="list-style-type: none"> A7 domain fully power gated. Wake-up only via MU_A (CM4 domain) or reset. 	MU_A ⁹ /Reset ⁴	60 µs

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1154)

Table 27-8. M4 power mode detail													
Power modes		HS RUN	RUN	VLPR	WAIT	PSTOP3	PSTOP2	PSTOP1	STOP	VLPS	LLS ¹	VLLS	BAT
Modules	Power State Power Domain	M4 supply on M4 RAM supply on DGO supply on FBB optional Allows DVS IO supplies on	M4 supply ON, M4 RAM supply ON, DGO supply ON, Allows DVS, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, RBB optional, IO supplies ON	M4 supply ON, M4 RAM supply ON, IO supplies ON, sys/bus clk ON	M4 supplies ON, IO supplies ON, sys clk OFF/bus clk ON	M4 supplies ON, IO supplies ON, sys clk OFF	M4 supplies ON, IO supplies ON, sys/bus clk OFF	M4 supply ON, M4 array supply ON, DGO supply ON, LVD protection, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 supply ON, reduced M4 RAM supply, reduced DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 Supply OFF, M4 RAM Supply ON, DGO supply ON, IO Supplies ON	M4 supply OFF, M4 RAM supply OFF, DGO supply OFF, IO supplies OFF

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1162)

4.3 System control for multicore operation

System controls on i.MX 7ULP must follow procedures described by individual peripherals below for multi-core operation. The device follows the concept of master core (M4) and slave core (A7). There are some peripherals that are multicore aware allowing both processors to access them. These peripherals typically contain controls that need dynamic changes throughout the applications. If these controls affect other peripherals or pins then the XRDC subsystem will pass ownership information to these multicore aware peripherals.

On the other hand, there are some peripherals that are typically configured once in the application. These peripherals are not multi-core aware and are expected to be configured by the master core.

4.3.1 Power modes, transition, wake-up, etc.

The Multicore System Mode Control (MSMC) module is used to control the power mode settings for each processor's domain. MSMC consists of SMC0 and SMC1, which are associated with M4 and A7 domains, respectively. The MSMC module works in conjunction with PMCs, RMCs and LLWU to facilitate power mode transitions.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 59)

28.1.1 Digital Power Management Controller (Digital PMC)

The Digital PMC module allows user software to control power modes of the chip and to optimize power consumption for the level of functionality needed. There are two instances of Digital PMC on this device, one for each main power domain.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1169)

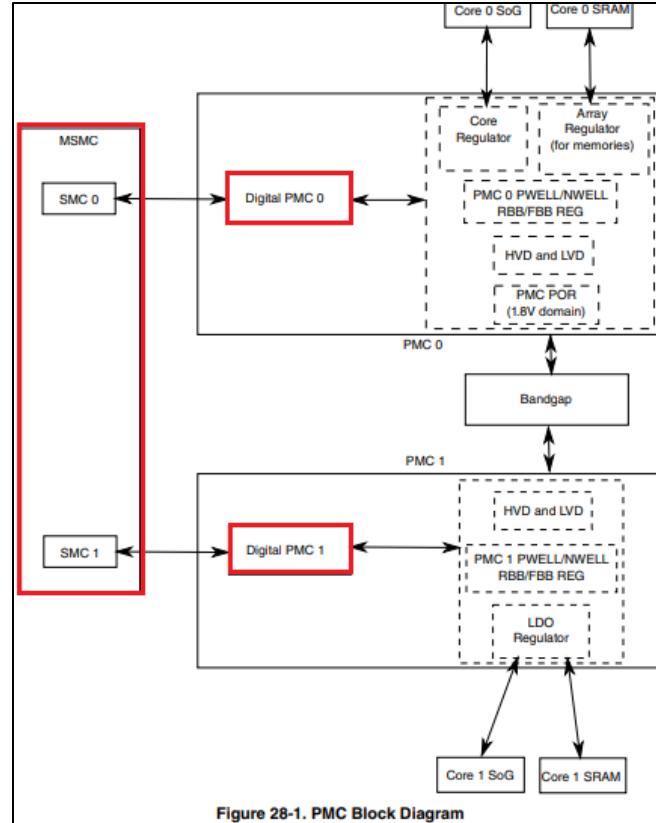
28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)



Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1173)

3 Overview of i.MX 7ULP power domains

The i.MX 7ULP has several power domains each containing multiple power supplies.

The i.MX 7ULP power architecture is organized in four main power domains:

- The **Real-Time Domain (RTD)** contains the Arm Cortex-M4 platform, multiple peripherals, system-level components and two GPIO ports (Ports A and B).
- The **Application Domain (AD)** contains the Arm Cortex-A7 platform, a 3D Graphics Processing Unit (3DGPU), a 2D Graphics Processing Unit (2DGPU), the LPDDR2/LPDDR3 interface (MMDC), the MIPI DSI display interface, multiple peripherals, and four GPIO ports (Ports C, D, E and F).
- The **DGO “Always-On” Domain** contains reset and system mode control logic, the Low-Leakage Wakeup Unit (LLWU), analog comparators and low-power timers.
- The **VBAT Domain** contains the Real-Time Clock (RTC) and Secure Non-Volatile Storage (SNVS) components.

In general, these domains are independent of each other. Multiple power modes are available in the Real-Time Domain and the Application Domain to optimize power consumption to the demands of the application at a given time. These modes optimize power consumption by reducing clock frequencies, reducing voltages, gating clocks and gating power supplies.

Source: <https://www.nxp.com/docs/en/application-note/AN12573.pdf> (Page 4)

1. i.MX 7ULP supports additional variant of WAIT mode called VLPS mode that allows peripheral operation at reduced frequency. See **MSMC** or **PMC** for details.
2. See **SLEEPDEEP mode**

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1154)

28. The method practiced using the accused products further comprises accessing body biasing voltage information corresponding to the power condition.

29. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP's processors support multiple power modes, including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode ("said power condition"). The body biasing voltage information for each processor and its different power modes is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively. Accordingly, the body biasing voltage information corresponding to the VLPS power mode is accessed from the corresponding register.

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biassing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), VLPS and LLS modes

1. All options for FBB/RBB are fully programmable

i.MX 7ULP Applications Processor Reference Manual, Rev. 0, 06/2019

NXP Semiconductors

1149

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VPLS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)

30. The method practiced using the accused products further comprises commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage corresponding to the body biasing voltage information corresponding to the power condition.

31. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode ("said power condition"). The body biasing voltage information for each processor is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively.

32. The PMC of each processor controls the body biasing voltage for that processor. Each PMC includes an Analog PMC, which consists of biasing regulators. The PMC can receive a voltage that is regulated using the back and forward biasing regulators ("voltage supply") for generating an appropriate body biasing voltage during different power modes. These body biasing voltages are then supplied to the VBBp and VBBn terminals ("body terminals").

33. Accordingly, the i.MX 7ULP Application Processor includes biasing regulators, which are coupled to the VBBp and VBBn terminals, that can be commanded to supply a body biasing voltage corresponding to a power mode, such as the VLPS mode ("said power condition").

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biassing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), VLPS and LLS modes

1. All options for FBB/RBB are fully programmable

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

28.4.11.3 Fields

Field	Function
31 PMC1Vsrc	<p>PMC 1 Voltage Source This flag indicates what is the voltage source selected to supply the PMC 1 and where the sense point of the PMC 1's LVD/HVD is placed.</p> <p>NOTE: The voltage source and LVD/HVD sense point of the PMC 1 are selected by the <code>PMC0_CTRL[LDOEN]</code> bit during a PMC 1 power-up. After that, the voltage source and sense point can be changed after a POR event only. For more information see Voltage Monitors.</p> <p>0b - The internal LDO supplies the PMC 1, the PMC 1's LVD/HVD sense point is at the supply of the LDO regulator.</p> <p>1b - The external PMIC supplies the PMC 1; the PMC 1's LVD/HVD sense point is at the pin connected to the PMIC.</p>

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Pages 1188-1189)

5.4.2 Analog power management controller (Analog PMC)

The Analog PMC consists of voltage/current references, core logic supply regulators, memory supply regulators, back and forward biasing regulators, monitors and power switches, etc. There are two Analog PMC subsystems, one associated with the M4 power domain and the other with the A7 power domain.

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 31)

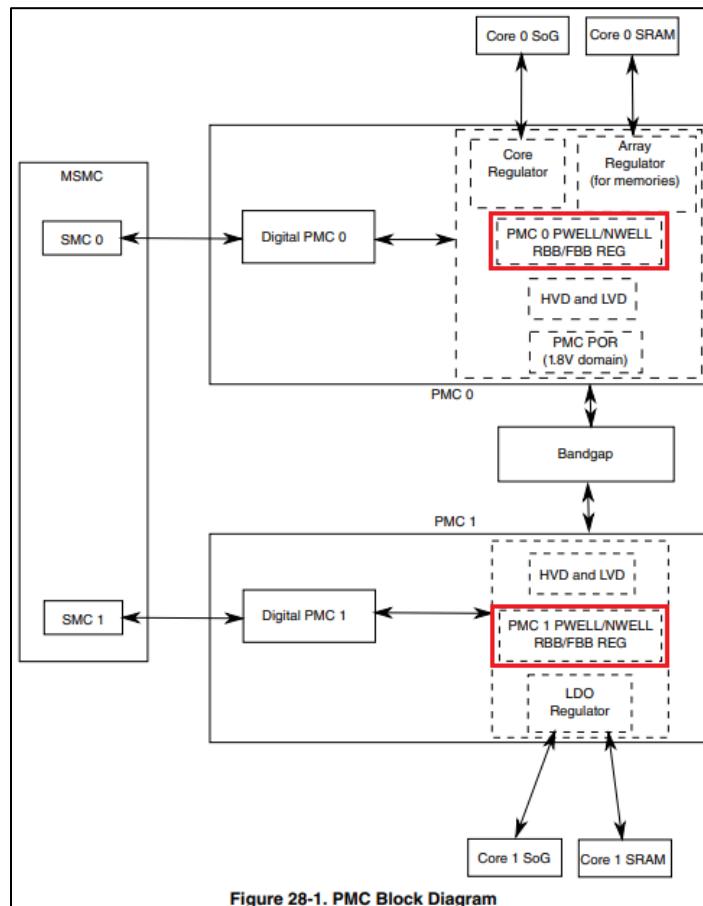


Figure 28-1. PMC Block Diagram

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1173)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

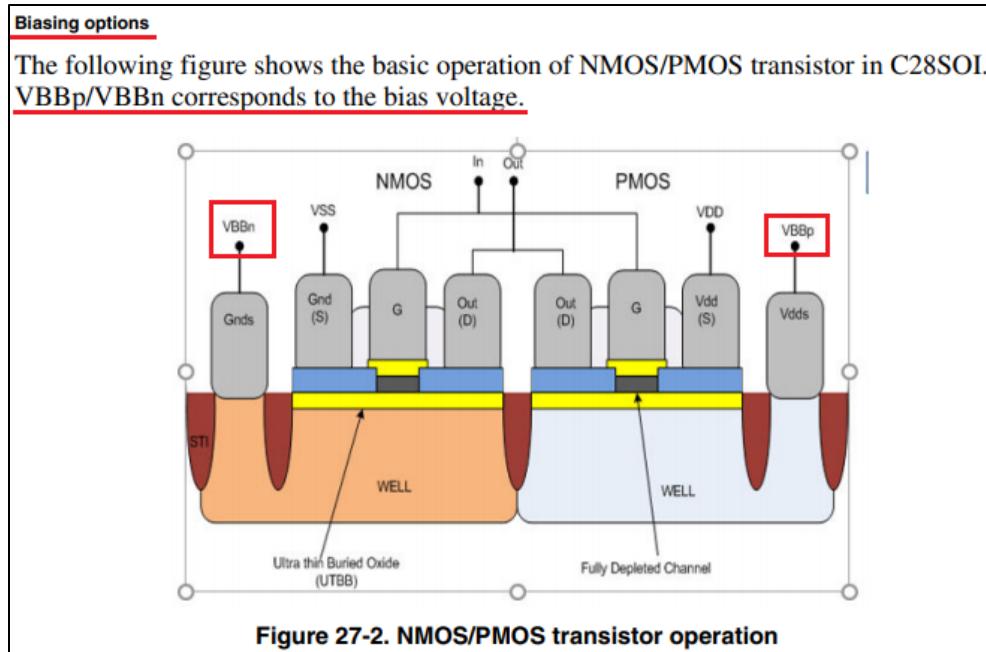
28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VLPS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)



Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

34. NXP has had knowledge of the '504 Patent at least as of January 28, 2014, when the '156 Patent, which states on its face that it is a continuation of the application leading to the '504 Patent, was cited by Freescale Semiconductor, Inc., a predecessor in interest to NXP, during prosecution of U.S. Patent Application No. 14/165,595. NXP employee, Meng Wang, who is the sole inventor listed on U.S. Patent Application No. 14/165,595, has had knowledge of the '504 Patent at least as of January 28, 2014.

35. Liberty Patents has been damaged as a result of the infringing conduct by NXP alleged above. Thus, NXP is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

36. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '504 Patent.

COUNT II

DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,127,156

37. On February 28, 2012, U.S. Patent No. 8,127,156 (“the ’156 Patent”) was duly and legally issued by the United States Patent and Trademark Office for an invention entitled “Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems.”

38. Liberty Patents is the owner of the ’156 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the ’156 Patent against infringers, and to collect damages for all relevant times.

39. NXP made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, NXP’s i.MX 7ULP Applications Processor and other products⁷ that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit (“accused products”):



i.MX 7ULP Family: Ultra-Low-Power with Graphics

Source: www.mouser.com/new/nxp-semiconductors/nxp-imx-7ulp-applications-processors/;
www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-7-processors/i-mx-7ulp-family-ultra-low-power-with-graphics:i.MX7ULP

⁷ See, e.g., NXP’s MCIMX7U5DVP07SC, MCIMX7U5DVK07SC, MCIMX7U3DVK07SC, MCIMX7U5CVP06SC, MCIMX7U3CVP06SC, MCIMX7U5DVP08SC, MCIMX7U3CVP06SD, MCIMX7U5CVP06SD, MCIMX7ULP-EVK, etc.

40. By doing so, NXP has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '156 Patent. NXP's infringement in this regard is ongoing.

41. NXP's i.MX 7ULP Applications Processor is an exemplary accused product.

42. NXP has infringed the '156 Patent by using the accused products and thereby practicing a method for determining a desirable power condition, of a set of power conditions, of a computer system comprising a microprocessor, wherein the set of power conditions comprises a power down state.

43. For example, NXP's i.MX 7ULP Applications Processor ("computer system") includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP's processors support multiple power modes, including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. The VLLS mode ("power down state") is one of the low power modes in which power to the processor is greatly reduced.

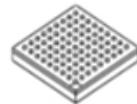
44. The system provides a Multicore System Mode Control (MSMC) module for controlling and changing the power modes of both processors. The MSMC module works with the Power Management Controller (PMC) of each processor. The MSMC module can determine a desirable power mode and send a command to the PMC to transition the processors to that desirable power mode.

i.MX 7ULP Applications

Processor—Consumer Products

The i.MX 7ULP product family members are optimized for power-sensitive applications benefiting from NXP's Heterogeneous Multicore Processing (HMP) architecture. Achieving an efficient balance between processing power and deterministic processing needs, the i.MX 7ULP is an asymmetric processor consisting of two separate processing domains: an application domain and a real-time domain. The application domain is built around an ARM® Cortex®-A7 processor with an ARM NEON™ SIMD engine and floating point unit (FPU) and is optimized for rich OS based applications. The real-time domain is built around an ARM Cortex-M4 processor (with FPU) optimized for lowest possible leakage. Both domains are completely independent, with separate power, clocking, and peripheral domains, but the bus fabric of each domain is tightly integrated for efficient communication. The part is streamlined to minimize pin count, enabling small packages and simple system integration.

MCIMX7U5DVP07SC
MCIMX7U5DVK07SC
MCIMX7U3DVK07SC



Plastic packages: BGA 14x14mm, 0.5mm pitch, and BGA 10 x 10 mm, 0.5 mm pitch

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 1)

The following table describes the power modes available to each core within the MCU.

Table 30-5. Power modes

Mode	Description
Run (RUN)	The core can be run at full frequency and all functionality is available. This mode is also referred to as Normal Run mode.
High Speed Run (HSRUN)	Provides the highest performance mode at the fastest supported frequency. The core, system, bus, and flash clock maximum frequencies are unrestricted in this mode. ¹
Wait (WAIT)	Allows a core to enter a static, low power state with instant wakeup time, while still allowing peripherals to operate with full functionality. The core clock is gated off. The system clock continues to operate. Bus clocks, if enabled, continue to operate.
Stop (STOP)	Allows a core and its peripherals to enter a static, low power state with relatively fast wakeup times, while still allowing peripherals to operate with full asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Very Low Power Run (VLPR)	Provides the lowest power operating mode to the core at a reduced frequency. The core, system, bus, and flash clock maximum frequencies are restricted in this mode. ¹
Very Low Power Wait (VLPW)	Allows a core to enter a static, very low power state, while still allowing peripherals to operate with full functionality at a reduced frequency. The core clock is gated off. The system, bus, and flash clocks continue to operate, although their maximum frequency is restricted. ¹
Very Low Power Stop (VLPS)	Allows a core and its peripherals to enter a static, very low power state with relatively fast wakeup times, while still allowing peripherals to operate with limited asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Low Leakage Stop (LLS)	Allows a core and its peripherals to enter a low leakage, power gated state with relatively fast wakeup times, while still retaining the state of all logic. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic and I/O are retained, with wakeup only supported via the LLWU, NMI or Reset pins.
Very Low Leakage Stop (VLLS)	Allows a core and its peripherals to enter a very low leakage, power gated state. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic is power gated, with wakeup only supported via the LLWU, NMI or Reset pins. I/O states are latched.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1242)

27.11 Power modes

27.11.1 A7 domain power

The A7 domain has multiple power modes. The following table describes the state of A7 domain in those modes.

Table 27-5. A7 power modes

A7 Power Mode	Description	Recovery Method	Recovery Time
<u>HSRUN</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • Allows FBB (optional) • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
RUN	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • FBB/RBB not allowed. • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
<u>VLPR</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Max Frequency restricted to FIRC (48 MHz). PLLs disabled. • Option to disable LVD/HVD 	N/A	N/A

Table continues on the next page...

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1153)

A7 Power Mode		Description		Recovery Method	Recovery Time
		<ul style="list-style-type: none"> DDR in self-refresh mode. DDR self-refresh must be done by software by writing to MMDC_MAPSR[LPMD] bit RBB not allowed 			
WAIT ^{1, 2}		<ul style="list-style-type: none"> Allows Peripherals to function while keeping core in sleep (clock-gated). A7 processor in Wait-for-Interrupt (WFI) state. 		Interrupt ³ /Reset ⁴	0 ns
STOP ⁵ /VLPS		<ul style="list-style-type: none"> IMX 7ULP is in static state with all registers retained with maintaining LVD protection. RBB only allowed in VLPS mode. FIRCCSR[FIRCLPEN] in the SCG module, keeps FIRC enabled in VLPS mode. LVDs could be turned off in VLPS mode. 		Interrupt/Reset ⁴	7 µs(STOP) and 23 µs (VLPS with RBB)/21.5 µs (VLPS without RBB) ⁶
LLS ⁷		<ul style="list-style-type: none"> A7 supply ON RBB is allowed LVD protection IO supplies ON A7 processor is in a wait-for-interrupt (WFI) state. The core clock is gated. Bus and DMA clocks are gated All peripheral clocks are gated. SRAM contents are retained. DDR can be in self-refresh 		Interrupt/Reset ⁴	Wake up time: 41.5 µs (LLS with RBB)/40 µs (LLS without RBB) ⁸
VLLS		<ul style="list-style-type: none"> A7 domain fully power gated. Wake-up only via MU_A (CM4 domain) or reset. DDR can be in self-refresh 		MU_A ⁹ /Reset ⁴	60 µs

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1154)

Table 27-8. <u>M4 power mode detail</u>													
Power modes		HS RUN	RUN	VLPR	WAIT	PSTOP3	PSTOP2	PSTOP1	STOP	VLPS	LLS ¹	VLLS	BAT
Modules	Power State Power Domain	M4 supply on M4 RAM supply on DGO supply on FBB optional Allows DVS IO supplies on	M4 supply ON, M4 RAM supply ON, DGO supply ON, RBB optional, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, RBB optional, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, IO supplies ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supply ON, M4 array supply ON, DGO supply ON, LVD protection, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 supply ON, reduced M4 RAM supply, reduced DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 Supply OFF, M4 RAM Supply ON, DGO supply ON, IO Supplies ON	M4 supply OFF, M4 RAM supply OFF, DGO supply OFF, IO supplies OFF

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1162)

30.5.4.4 Very Low Leakage Stop (VLLS) modes

VLLS mode is designed to allow a core and its system to enter a very low leakage, power gated state. Refer to the device's Power Management chapter for peripheral, I/O, and memory operation in VLLS mode and see the PMC chapter for additional power options available in this mode.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1292)

Table 35-2. A7 system reset sources

Reset source	Reset name	Comments
Power-On-Reset	POR_A7	—
Reset pin (External)	RESET_A7_b	—
System_Reset_M4	SYS_RESET_M4	ORed version of all system reset sources from M4
WDOG (A7)	WDOG_A7_RST	—
Core Software Reset	SW_RST_A7	Software reset initiated by CA7
CPU Exception	CPU_EXP_A7	—
Secure WDOG	WDOG_RST	Optional reset
Stop Mode Ack Error	STOP_ACK_A7	—
Power Down Wakeup	VLLS_WAKEUP_A7	Wake-up from VLLS/Power down mode via MU

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1457)

4.3 System control for multicore operation

System controls on i.MX 7ULP must follow procedures described by individual peripherals below for multi-core operation. The device follows the concept of master core (M4) and slave core (A7). There are some peripherals that are multicore aware allowing both processors to access them. These peripherals typically contain controls that need dynamic changes throughout the applications. If these controls affect other peripherals or pins then the XRDC subsystem will pass ownership information to these multicore aware peripherals.

On the other hand, there are some peripherals that are typically configured once in the application. These peripherals are not multi-core aware and are expected to be configured by the master core.

4.3.1 Power modes, transition, wake-up, etc.

The Multicore System Mode Control (MSMC) module is used to control the power mode settings for each processor's domain. MSMC consists of SMC0 and SMC1, which are associated with M4 and A7 domains, respectively. The MSMC module works in conjunction with PMCs, RMCs and LLWU to facilitate power mode transitions.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 59)

28.1.1 Digital Power Management Controller (Digital PMC)

The Digital PMC module allows user software to control power modes of the chip and to optimize power consumption for the level of functionality needed. There are two instances of Digital PMC on this device, one for each main power domain.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1169)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

3 Overview of i.MX 7ULP power domains

The i.MX 7ULP has several power domains each containing multiple power supplies.

The i.MX 7ULP power architecture is organized in four main power domains:

- The **Real-Time Domain (RTD)** contains the Arm Cortex-M4 platform, multiple peripherals, system-level components and two GPIO ports (Ports A and B).
- The **Application Domain (AD)** contains the Arm Cortex-A7 platform, a 3D Graphics Processing Unit (3DGPU), a 2D Graphics Processing Unit (2DGPU), the LPDDR2/LPDDR3 interface (MMDC), the MIPI DSI display interface, multiple peripherals, and four GPIO ports (Ports C, D, E and F).
- The **DGO "Always-On" Domain** contains reset and system mode control logic, the Low-Leakage Wakeup Unit (LLWU), analog comparators and low-power timers.
- The **VBAT Domain** contains the Real-Time Clock (RTC) and Secure Non-Volatile Storage (SNVS) components.

In general, these domains are independent of each other. Multiple power modes are available in the Real-Time Domain and the Application Domain to optimize power consumption to the demands of the application at a given time. These modes optimize power consumption by reducing clock frequencies, reducing voltages, gating clocks and gating power supplies.

Source: <https://www.nxp.com/docs/en/application-note/AN12573.pdf> (Page 4)

45. The method practiced using the accused products further comprises accessing body biasing voltage information corresponding to the power condition.

46. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing.

Both of the i.MX 7ULP's processors support multiple power modes, including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode ("said power condition"). The body biasing voltage information for each processor and its different power modes is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively. Accordingly, the body biasing voltage information corresponding to the VLPS power mode is accessed from the corresponding register.

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Blasing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), <u>VLPS</u> and LLS modes

1. All options for FBB/RBB are fully programmable

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Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

Real Time Domain (M4 domain) PMC 0 Register Configuration Requirements				
PMC0_HSRUN [COREREGVL]	PMC0 HSRUN mode LDO configuration requirements	HSRUN mode FBB=0.3 V	—	101010b (1.05 V)
PMC0_RUN [COREREGVL]	PMC0 RUN mode LDO configuration requirements	RUN mode No bias	—	011100b (0.90 V)
PMC0_VLPR [COREREGVL]	PMC0 VLPR mode LDO configuration requirements	VLPR mode	—	011100b (0.90 V)
PMC0_STOP [COREREGVL]	PMC0 STOP mode LDO configuration requirements	STOP mode	—	011100b (0.90 V)
PMC0_VLPS [COREREGVL]	PMC0 VLPS mode LDO configuration requirements	VLPS mode	—	011100b (0.90 V)
PMC0_LLS [COREREGVL]	PMC0 LLS mode LDO configuration requirements	LLS mode	—	001101b (0.73V)
RDIG0	External board routing impedance from VDD_PMC11_DIG0_CAP to VDD_DIG0	—	—	—

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 34)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (In bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (In bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IM.X7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBPLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VLPS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)

47. The method practiced using the accused products further comprises commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage corresponding to the body biasing voltage information corresponding to the power condition.

48. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode ("said power condition"). The body biasing voltage information for each processor is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively.

49. The PMC of each processor controls the body biasing voltage for that processor. Each PMC includes an Analog PMC, which consists of biasing regulators. The PMC can receive a voltage that is regulated using the back and forward biasing regulators ("voltage supply") for generating an appropriate body biasing voltage during different power modes. These body biasing voltages are then supplied to the VBBp and VBBn terminals ("body terminals").

50. Accordingly, the i.MX 7ULP Application Processor includes biasing regulators, which are coupled to the VBBp and VBBn terminals, that can be commanded to supply a body biasing voltage corresponding to a power mode, such as the VLPS mode ("said power condition").

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biasing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), <u>VLPS</u> and LLS modes

1. All options for FBB/RBB are fully programmable

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Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

28.4.11.3 Fields

Field	Function
31 PMC1VSR	<p>PMC 1 Voltage Source This flag indicates what is the voltage source selected to supply the PMC 1 and where the sense point of the PMC 1's LVD/HVD is placed.</p> <p>NOTE: The voltage source and LVD/HVD sense point of the PMC 1 are selected by the PMC0_CTRL[LDOEN] bit during a PMC 1 power-up. After that, the voltage source and sense point can be changed after a POR event only. For more information see Voltage Monitors .</p> <p>0b - The internal LDO supplies the PMC 1, the PMC 1's LVD/HVD sense point is at the supply of the LDO regulator.</p> <p>1b - The external PMIC supplies the PMC 1; the PMC 1's LVD/HVD sense point is at the pin connected to the PMIC.</p>

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Pages 1188-1189)

5.4.2 Analog power management controller (Analog PMC)

The Analog PMC consists of voltage/current references, core logic supply regulators, memory supply regulators, back and forward biasing regulators, monitors and power switches, etc. There are two Analog PMC subsystems, one associated with the M4 power domain and the other with the A7 power domain.

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 31)

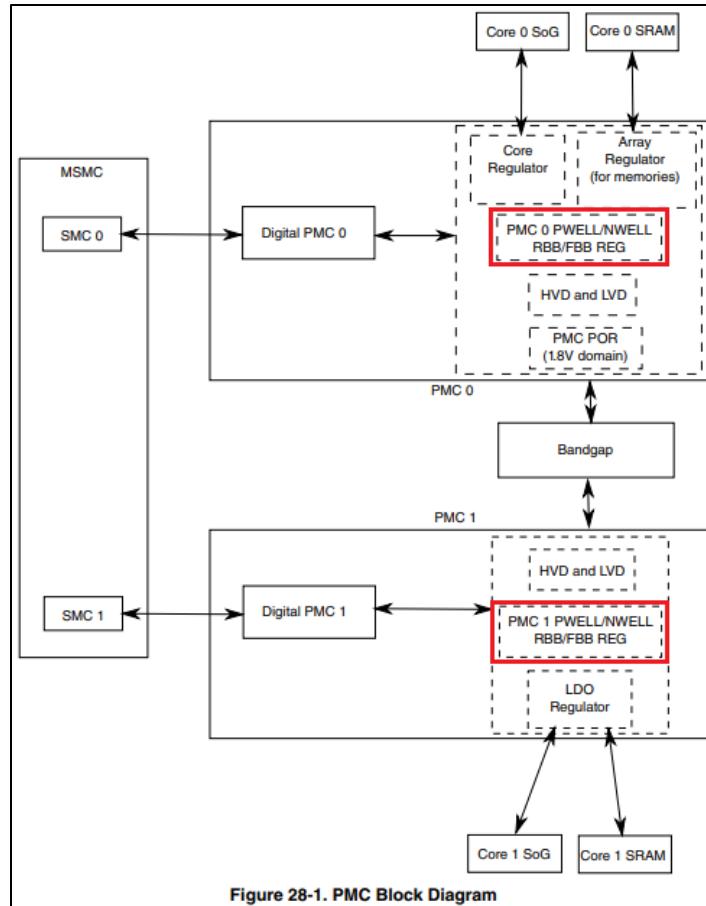


Figure 28-1. PMC Block Diagram

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1173)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

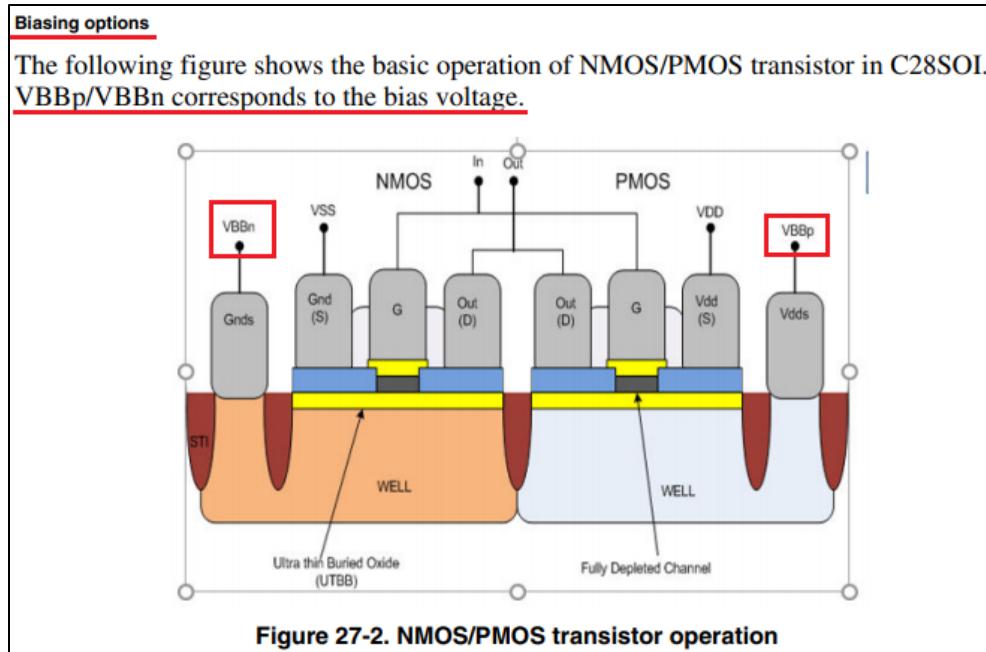
28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VLPS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)



Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

51. NXP has had knowledge of the '156 Patent at least as of January 28, 2014, when the '156 Patent was cited by Freescale Semiconductor, Inc., a predecessor in interest to NXP, during prosecution of U.S. Patent Application No. 14/165,595. NXP employee, Meng Wang, who is the sole inventor listed on U.S. Patent Application No. 14/165,595, has had knowledge of the '156 Patent at least as of January 28, 2014.

52. Liberty Patents has been damaged as a result of the infringing conduct by NXP alleged above. Thus, NXP is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

53. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '156 Patent.

COUNT III

DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,458,496

54. On June 4, 2013, U.S. Patent No. 8,458,496 (“the ’496 Patent”) was duly and legally issued by the United States Patent and Trademark Office for an invention entitled “Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems.”

55. Liberty Patents is the owner of the ’496 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the ’496 Patent against infringers, and to collect damages for all relevant times.

56. NXP made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, NXP’s i.MX 7ULP Applications Processor and other products⁸ that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit (“accused products”):



i.MX 7ULP Family: Ultra-Low-Power with Graphics

Source: www.mouser.com/new/nxp-semiconductors/nxp-imx-7ulp-applications-processors/;
www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-7-processors/i-mx-7ulp-family-ultra-low-power-with-graphics:i.MX7ULP

⁸ See, e.g., NXP’s MCIMX7U5DVP07SC, MCIMX7U5DVK07SC, MCIMX7U3DVK07SC, MCIMX7U5CVP06SC, MCIMX7U3CVP06SC, MCIMX7U5DVP08SC, MCIMX7U3CVP06SD, MCIMX7U5CVP06SD, MCIMX7ULP-EVK, etc.

57. By doing so, NXP has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '496 Patent. NXP's infringement in this regard is ongoing.

58. NXP's i.MX 7ULP Applications Processor is an exemplary accused product.

59. NXP's i.MX 7ULP Applications Processor includes means for determining a particular power condition, of a set of power conditions, of a computer system comprising a microprocessor, wherein the set of power conditions comprises a power down state.

60. For example, NXP's i.MX 7ULP Applications Processor ("computer system") includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP's processors support multiple power modes ("a set of power conditions"), including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. The VLLS mode ("a power down state") is one of the low power modes in which power to the processor is greatly reduced.

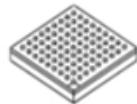
61. The system provides a Multicore System Mode Control (MSMC) module for controlling and changing the power modes of both processors. The MSMC module works with the Power Management Controller (PMC) of each processor to change the power modes of the processor. The MSMC module can determine a desirable power mode and send a command to the PMC to transition the processors to that desirable power mode.

i.MX 7ULP Applications

Processor—Consumer Products

The i.MX 7ULP product family members are optimized for power-sensitive applications benefiting from NXP's Heterogeneous Multicore Processing (HMP) architecture. Achieving an efficient balance between processing power and deterministic processing needs, the i.MX 7ULP is an asymmetric processor consisting of two separate processing domains: an application domain and a real-time domain. The application domain is built around an ARM® Cortex®-A7 processor with an ARM NEON™ SIMD engine and floating point unit (FPU) and is optimized for rich OS based applications. The real-time domain is built around an ARM Cortex-M4 processor (with FPU) optimized for lowest possible leakage. Both domains are completely independent, with separate power, clocking, and peripheral domains, but the bus fabric of each domain is tightly integrated for efficient communication. The part is streamlined to minimize pin count, enabling small packages and simple system integration.

MCIMX7U5DVP07SC
MCIMX7U5DVK07SC
MCIMX7U3DVK07SC



Plastic packages: BGA 14x14mm, 0.5mm pitch, and BGA 10 x 10 mm, 0.5 mm pitch

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 1)

The following table describes the power modes available to each core within the MCU.

Table 30-5. Power modes

Mode	Description
Run (RUN)	The core can be run at full frequency and all functionality is available. This mode is also referred to as Normal Run mode.
High Speed Run (HSRUN)	Provides the highest performance mode at the fastest supported frequency. The core, system, bus, and flash clock maximum frequencies are unrestricted in this mode. ¹
Wait (WAIT)	Allows a core to enter a static, low power state with instant wakeup time, while still allowing peripherals to operate with full functionality. The core clock is gated off. The system clock continues to operate. Bus clocks, if enabled, continue to operate.
Stop (STOP)	Allows a core and its peripherals to enter a static, low power state with relatively fast wakeup times, while still allowing peripherals to operate with full asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Very Low Power Run (VLPR)	Provides the lowest power operating mode to the core at a reduced frequency. The core, system, bus, and flash clock maximum frequencies are restricted in this mode. ¹
Very Low Power Wait (VLPW)	Allows a core to enter a static, very low power state, while still allowing peripherals to operate with full functionality at a reduced frequency. The core clock is gated off. The system, bus, and flash clocks continue to operate, although their maximum frequency is restricted. ¹
Very Low Power Stop (VLPS)	Allows a core and its peripherals to enter a static, very low power state with relatively fast wakeup times, while still allowing peripherals to operate with limited asynchronous functionality. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.
Low Leakage Stop (LLS)	Allows a core and its peripherals to enter a low leakage, power gated state with relatively fast wakeup times, while still retaining the state of all logic. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic and I/O are retained, with wakeup only supported via the LLWU, NMI or Reset pins.
Very Low Leakage Stop (VLLS)	Allows a core and its peripherals to enter a very low leakage, power gated state. The core clock is gated off. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid. Logic is power gated, with wakeup only supported via the LLWU, NMI or Reset pins. I/O states are latched.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1242)

27.11 Power modes

27.11.1 A7 domain power

The A7 domain has multiple power modes. The following table describes the state of A7 domain in those modes.

Table 27-5. A7 power modes

A7 Power Mode	Description	Recovery Method	Recovery Time
<u>HSRUN</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • Allows FBB (optional) • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
RUN	<ul style="list-style-type: none"> • All logic is functional in this mode. • Bus clock and peripherals functional. • FBB/RBB not allowed. • Allows Dynamic Voltage Scaling(DVS) 	N/A	N/A
<u>VLPR</u>	<ul style="list-style-type: none"> • All logic is functional in this mode. • Max Frequency restricted to FIRC (48 MHz). PLLs disabled. • Option to disable LVD/HVD 	N/A	N/A

Table continues on the next page...

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1153)

A7 Power Mode		Description		Recovery Method	Recovery Time
		<ul style="list-style-type: none"> DDR in self-refresh mode. DDR self-refresh must be done by software by writing to MMDC_MAPSR[LPMD] bit RBB not allowed 			
WAIT ^{1, 2}		<ul style="list-style-type: none"> Allows Peripherals to function while keeping core in sleep (clock-gated). A7 processor in Wait-for-Interrupt (WFI) state. 		Interrupt ³ /Reset ⁴	0 ns
STOP ⁵ /VLPS		<ul style="list-style-type: none"> IMX 7ULP is in static state with all registers retained with maintaining LVD protection. RBB only allowed in VLPS mode. FIRCCSR[FIRCLPEN] in the SCG module, keeps FIRC enabled in VLPS mode. LVDs could be turned off in VLPS mode. 		Interrupt/Reset ⁴	7 µs(STOP) and 23 µs (VLPS with RBB)/21.5 µs (VLPS without RBB) ⁶
LLS ⁷		<ul style="list-style-type: none"> A7 supply ON RBB is allowed LVD protection IO supplies ON A7 processor is in a wait-for-interrupt (WFI) state. The core clock is gated. Bus and DMA clocks are gated All peripheral clocks are gated. SRAM contents are retained. DDR can be in self-refresh 		Interrupt/Reset ⁴	Wake up time: 41.5 µs (LLS with RBB)/40 µs (LLS without RBB) ⁸
VLLS		<ul style="list-style-type: none"> A7 domain fully power gated. Wake-up only via MU_A (CM4 domain) or reset. DDR can be in self-refresh 		MU_A ⁹ /Reset ⁴	60 µs

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1154)

Table 27-8. <u>M4 power mode detail</u>													
Power modes		HS RUN	RUN	VLPR	WAIT	PSTOP3	PSTOP2	PSTOP1	STOP	VLPS	LLS ¹	VLLS	BAT
Modules	Power State Power Domain	M4 supply on M4 RAM supply on DGO supply on FBB optional Allows DVS IO supplies on	M4 supply ON, M4 RAM supply ON, DGO supply ON, RBB optional, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, RBB optional, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, IO supplies ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supplies ON, IO supplies ON, sysclk ON	M4 supply ON, M4 array supply ON, DGO supply ON, LVD protection, IO supplies ON	M4 supply ON, M4 RAM supply ON, DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 supply ON, reduced M4 RAM supply, reduced DGO supply ON, LVD protection, RBB optional, IO supplies ON	M4 Supply OFF, M4 RAM Supply ON, DGO supply ON, IO Supplies ON	M4 supply OFF, M4 RAM supply OFF, DGO supply OFF, IO supplies OFF

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1162)

30.5.4.4 Very Low Leakage Stop (VLLS) modes

VLLS mode is designed to allow a core and its system to enter a very low leakage, power gated state. Refer to the device's Power Management chapter for peripheral, I/O, and memory operation in VLLS mode and see the PMC chapter for additional power options available in this mode.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1292)

Table 35-2. A7 system reset sources

Reset source	Reset name	Comments
Power-On-Reset	POR_A7	—
Reset pin (External)	RESET_A7_b	—
System_Reset_M4	SYS_RESET_M4	Optional version of all system reset sources from M4
WDOG (A7)	WDOG_A7_RST	—
Core Software Reset	SW_RST_A7	Software reset initiated by CA7
CPU Exception	CPU_EXP_A7	—
Secure WDOG	WDOG_RST	Optional reset
Stop Mode Ack Error	STOP_ACK_A7	—
Power Down Wakeup	VLLS_WAKEUP_A7	Wake-up from VLLS/Power down mode via MU

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1457)

4.3 System control for multicore operation

System controls on i.MX 7ULP must follow procedures described by individual peripherals below for multi-core operation. The device follows the concept of master core (M4) and slave core (A7). There are some peripherals that are multicore aware allowing both processors to access them. These peripherals typically contain controls that need dynamic changes throughout the applications. If these controls affect other peripherals or pins then the XRDC subsystem will pass ownership information to these multicore aware peripherals.

On the other hand, there are some peripherals that are typically configured once in the application. These peripherals are not multi-core aware and are expected to be configured by the master core.

4.3.1 Power modes, transition, wake-up, etc.

The Multicore System Mode Control (MSMC) module is used to control the power mode settings for each processor's domain. MSMC consists of SMC0 and SMC1, which are associated with M4 and A7 domains, respectively. The MSMC module works in conjunction with PMCs, RMCs and LLWU to facilitate power mode transitions.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 59)

28.1.1 Digital Power Management Controller (Digital PMC)

The Digital PMC module allows user software to control power modes of the chip and to optimize power consumption for the level of functionality needed. There are two instances of Digital PMC on this device, one for each main power domain.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1169)

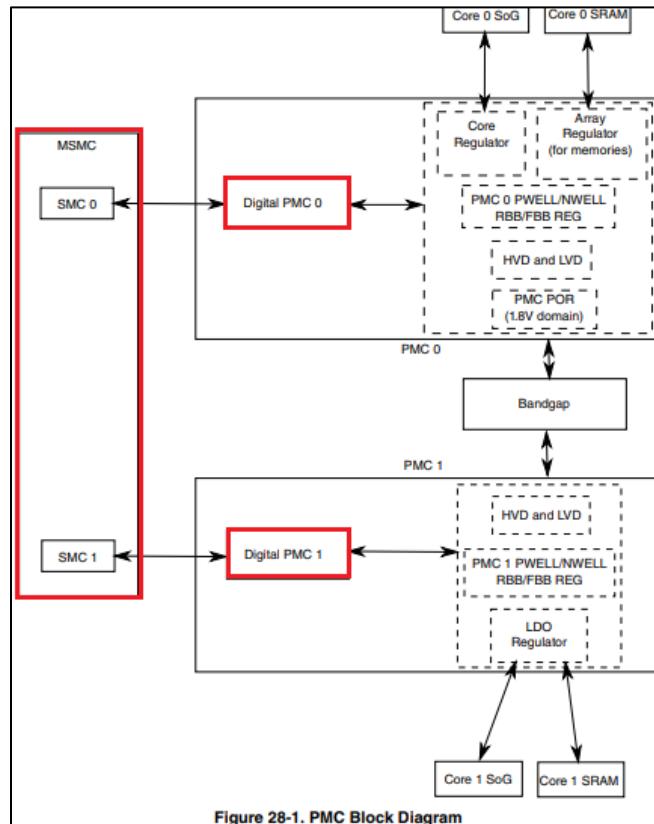
28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)



Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1173)

3 Overview of i.MX 7ULP power domains

The i.MX 7ULP has several power domains each containing multiple power supplies.

The i.MX 7ULP power architecture is organized in four main power domains:

- The **Real-Time Domain (RTD)** contains the Arm Cortex-M4 platform, multiple peripherals, system-level components and two GPIO ports (Ports A and B).
- The **Application Domain (AD)** contains the Arm Cortex-A7 platform, a 3D Graphics Processing Unit (3DGPU), a 2D Graphics Processing Unit (2DGPU), the LPDDR2/LPDDR3 interface (MMDC), the MIPI DSI display interface, multiple peripherals, and four GPIO ports (Ports C, D, E and F).
- The **DGO “Always-On” Domain** contains reset and system mode control logic, the Low-Leakage Wakeup Unit (LLWU), analog comparators and low-power timers.
- The **VBAT Domain** contains the Real-Time Clock (RTC) and Secure Non-Volatile Storage (SNVS) components.

In general, these domains are independent of each other. Multiple power modes are available in the Real-Time Domain and the Application Domain to optimize power consumption to the demands of the application at a given time. These modes optimize power consumption by reducing clock frequencies, reducing voltages, gating clocks and gating power supplies.

Source: <https://www.nxp.com/docs/en/application-note/AN12573.pdf> (Page 4)

62. NXP’s i.MX 7ULP Applications Processor includes means for accessing body biasing voltage information corresponding to the particular power condition.

63. For example, NXP’s i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. Both of the i.MX 7ULP’s processors support multiple power modes, including HSRUN (High Speed RUN), VLPR (Very Low Power Run), VLPS (Very Low Power Stop), LLS (Low Leakage Stop), etc. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode (“said particular power condition”). The body biasing voltage information for each processor and its different power modes is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively. Accordingly, the i.MX 7ULP Applications Processor includes means for accessing the body biasing voltage information corresponding to the VLPS power mode from the corresponding register.

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biasing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), <u>VLPS</u> and LLS modes

1. All options for FBB/RBB are fully programmable

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NXP Semiconductors

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Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

Real Time Domain (M4 domain) PMC 0 Register Configuration Requirements				
PMC0_HSRUN [COREREGVL]	PMC0 HSRUN mode LDO configuration requirements	HSRUN mode FBB=0.3 V	—	101010b (1.05 V)
PMC0_RUN [COREREGVL]	PMC0 RUN mode LDO configuration requirements	RUN mode No bias	—	011100b (0.90 V)
PMC0_VLPR [COREREGVL]	PMC0 VLPR mode LDO configuration requirements	VLPR mode	—	011100b (0.90 V)
PMC0_STOP [COREREGVL]	PMC0 STOP mode LDO configuration requirements	STOP mode	—	011100b (0.90 V)
PMC0_VLPS [COREREGVL]	PMC0 VLPS mode LDO configuration requirements	VLPS mode	—	011100b (0.90 V)
PMC0_LLS [COREREGVL]	PMC0 LLS mode LDO configuration requirements	LLS mode	—	001101b (0.73V)
RDIG0	External board routing impedance from VDD_PMC11_DIG0_CAP to VDD_DIG0	—	—	—

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 34)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VPLS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)

64. NXP's i.MX 7ULP Applications Processor includes means for commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage

corresponding to the body biasing voltage information corresponding to the particular power condition.

65. For example, NXP's i.MX 7ULP Applications Processor includes two separate processors—one for application domain processing and another for real-time domain processing. A body biasing voltage is applied during different power modes of each processor, e.g., during the VLPS mode ("said particular power condition"). The body biasing voltage information for each processor is stored in the PMC0_BCTRL and PMC1_BCTRL registers, respectively.

66. The PMC of each processor controls the body biasing voltage for that processor. Each PMC includes an Analog PMC, which consists of biasing regulators. The PMC can receive a voltage that is regulated using the back and forward biasing regulators ("voltage supply") for generating an appropriate body biasing voltage during different power modes. These body biasing voltages are then supplied to the VBBp and VBBn terminals ("body terminals"). Accordingly, the i.MX 7ULP Applications Processor includes means for commanding the biasing regulators to generate body biasing voltage that corresponds to a particular power mode, such as the VLPS mode.

27.8 Biasing options

i.MX 7ULP supports both Forward and Reverse bias; however only variants of options would be available based on power modes.

The following table shows applicable power modes for both the biasing options.

Table 27-3. Biasing options

Biassing Options ¹	Bias Voltage Range (Typical)	Applicable Power modes
Forward Body Bias (FBB)	50 mV to 350 mV, with 50 mV voltage steps	HSRUN Mode
Reverse Body Bias(RBB)	500 mV to 1.3 V, with 100 mV voltage steps	VLPR (CM4 domain only), <u>VLPS</u> and LLS modes

1. All options for FBB/RBB are fully programmable

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1149)

The following table shows the valid RBB/FBB combinations for i.MX 7ULP

Table 27-4. Valid RBB/FBB combinations for i.MX 7ULP

A7 Domain	M4 Domain	Valid i.MX 7ULP use-case	Applicable A7/M4 Power mode
No Biasing	No Biasing	YES	No Restriction
FBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (RUN Mode)
FBB	FBB	YES	<ul style="list-style-type: none"> • A7 (HSRUN Mode) • M4 (HSRUN Mode)
FBB	RBB	YES	N/A
Power Gated	FBB	YES	M4 (HSRUN Mode)
Power Gated	RBB	YES	M4 (VLPR, VLPS, LLS modes)
RBB	No Biasing	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (RUN mode)
RBB	FBB	YES	N/A
RBB	RBB	YES	<ul style="list-style-type: none"> • A7 (VLPS, LLS modes) • M4 (VLPR, VLPS, LLS modes)

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

28.2 Introduction

The Power Management Controller (PMC) can be divided into two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0 SoG supply, the Core 0 SRAMs power modes and the Core 0 biasing. The PMC 1 controls the Core 1 SoG supply, the Core 1 SRAMs power modes and the Core 1 biasing. The PMC also has voltage monitors in both power domains (PMC 0 and PMC 1).

Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features will be enabled or disabled by each power mode.

The Figure 28-1 shows the PMC block diagram.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1172)

28.4.11.3 Fields

Field	Function
31 PMC1Vsrc	<p>PMC 1 Voltage Source This flag indicates what is the voltage source selected to supply the PMC 1 and where the sense point of the PMC 1's LVD/HVD is placed.</p> <p>NOTE: The voltage source and LVD/HVD sense point of the PMC 1 are selected by the PMC0_CTRL[LDOEN] bit during a PMC 1 power-up. After that, the voltage source and sense point can be changed after a POR event only. For more information see Voltage Monitors .</p> <p>0b - The internal LDO supplies the PMC 1, the PMC 1's LVD/HVD sense point is at the supply of the LDO regulator.</p> <p>1b - The external PMIC supplies the PMC 1; the PMC 1's LVD/HVD sense point is at the pin connected to the PMIC.</p>

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Pages 1188-1189)

5.4.2 Analog power management controller (Analog PMC)

The Analog PMC consists of voltage/current references, core logic supply regulators, memory supply regulators, back and forward biasing regulators, monitors and power switches, etc. There are two Analog PMC subsystems, one associated with the M4 power domain and the other with the A7 power domain.

Source: <https://www.nxp.com/docs/en/data-sheet/IMX7ULPCEC.pdf> (Page 31)

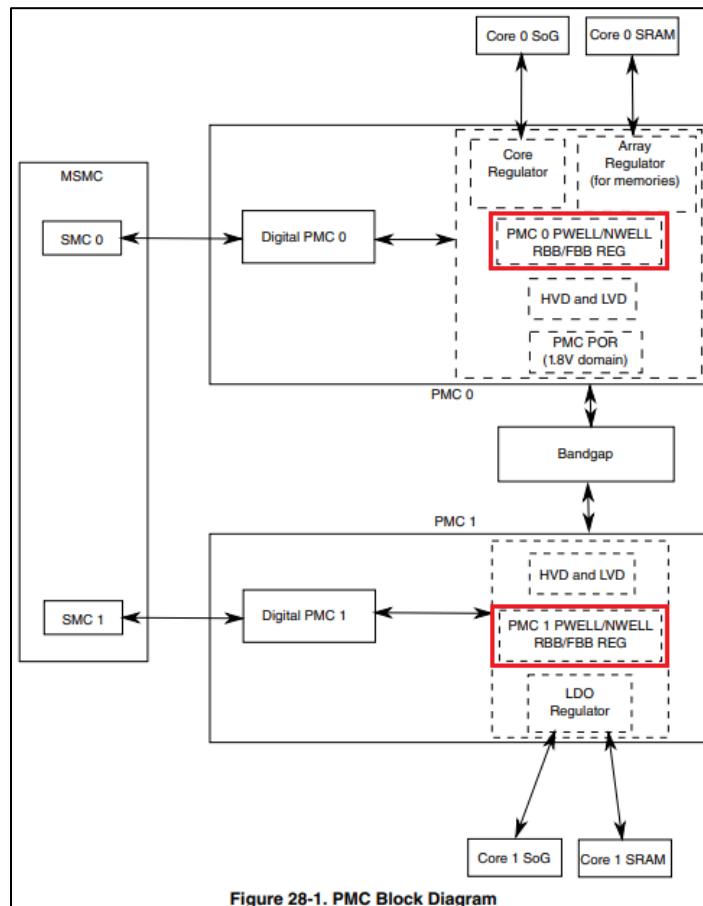


Figure 28-1. PMC Block Diagram

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1173)

28.4.1 PMC0 memory map

PMC0 base address: 410A_1000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 0 Version register (VERID)	32	RO	0000_0000h
4h	PMC 0 Power Mode Status register (PM_STAT)	32	RO	0001_0001h
8h	PMC 0 HSRUN mode register (HSRUN)	32	RW	001C_0000h
Ch	PMC 0 RUN mode register (RUN)	32	RW	001C_0000h
10h	PMC 0 VLPR mode register (VLPR)	32	RW	000A_0000h
14h	PMC 0 STOP mode register (STOP)	32	RW	001C_0000h
18h	PMC 0 VLPS mode register (VLPS)	32	RW	000A_0000h
1Ch	PMC 0 LLS mode register (LLS)	32	RW	000A_0000h
20h	PMC 0 VLLS mode register (VLLS)	32	RW	0000_0002h
24h	PMC 0 Status register (STATUS)	32	RO	8000_0000h
28h	PMC 0 Control register (CTRL)	32	RW	Table 28-4
30h	PMC 0 Analog Core Control register (ACTRL)	32	RW	Table 28-4
38h	PMC 0 Biasing Control register (BCTRL)	32	RW	Table 28-4
48h	PMC 0 SRAMs Control 0 register (SRAMCTRL_0)	32	RW	0000_0000h
4Ch	PMC 0 SRAMs Control 1 register (SRAMCTRL_1)	32	RW	0000_0000h
50h	PMC 0 SRAMs Control 2 register (SRAMCTRL_2)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1175)

28.5.1 PMC1 memory map

PMC1 base address: 4040_0000h

Offset	Register	Width (in bits)	Access	Reset value
0h	PMC 1 Version register (VERID)	32	RO	0000_0000h
4h	PMC 1 HSRUN mode register (HSRUN)	32	RW	0028_0000h
8h	PMC 1 RUN mode register (RUN)	32	RW	0028_0000h
Ch	PMC 1 VLPR mode register (VLPR)	32	RW	000A_0000h
10h	PMC 1 STOP mode register (STOP)	32	RW	0028_0000h
14h	PMC 1 VLPS mode register (VLPS)	32	RW	000A_0000h
18h	PMC 1 LLS mode register (LLS)	32	RW	000A_0000h
1Ch	PMC 1 VLLS mode register (VLLS)	32	RW	0000_0000h
20h	PMC 1 Status register (STATUS)	32	RO	0000_0000h
24h	PMC 1 Control register (CTRL)	32	RW	0000_0000h
34h	PMC 1 Biasing Control register (BCTRL)	32	RW	Table 28-4
44h	PMC 1 SRAMs Control register (SRAMCTRL)	32	RW	0000_0000h

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1200).

15	RBBPDDIS	RBB Pull-down Disable Selects if RBB pull-down will be disabled in a transition to VLPR. 0b - RBB pull-down is enabled. 1b - RBB pull-down is disabled.
14-12	—	Reserved field
11-8	RBBLEVEL	RBB P-Well Voltage Level Selects the voltage level of the RBB P-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBLEVEL must be programmed to voltage level at -1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at -0.5V. 0001b - Voltage level at -0.6V. 0010b - Voltage level at -0.7V. 0011b - Voltage level at -0.8V. 0100b - Voltage level at -0.9V. 0101b - Voltage level at -1.0V. 0110b - Voltage level at -1.1V. 0111b - Voltage level at -1.2V. 1000b - Voltage level at -1.3V.
7-4	—	Reserved field
3-0	RBBNLEVEL	RBB N-Well Voltage Level Selects the voltage level of the RBB N-Well regulator. Values related to the domain voltage source. 100 mV steps. For more information see Enable or Configure RBB . NOTE: RBBNLEVEL must be programmed to voltage level at 1.0v (0101b) for i.MX 7ULP. 0000b - Voltage level at 0.5V. 0001b - Voltage level at 0.6V. 0010b - Voltage level at 0.7V. 0011b - Voltage level at 0.8V. 0100b - Voltage level at 0.9V. 0101b - Voltage level at 1.0V. 0110b - Voltage level at 1.1V. 0111b - Voltage level at 1.2V. 1000b - Voltage level at 1.3V.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1196)

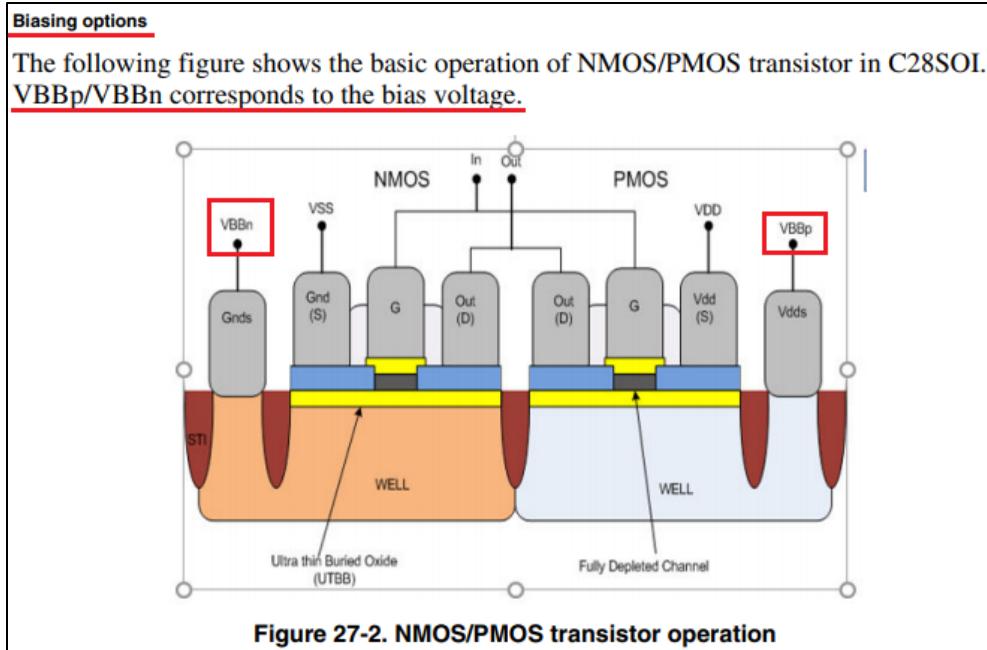
28.6.10.6 Enable or Configure RBB

To enable or configure RBB, i.e. to change the voltage level or enable/disable pull-down, the procedure is following:

- Go to RUN mode.
- Change the value of RBBNLEVEL or RBBLEVEL bitfields in PMC0_BCTRL register if required.
- Assert RBBPDDIS bitfield in PMC0_BCTRL register if required.
- Assert RBBEN bit of the respective low power mode register (PMCx_VLPR, PMCx_LLS or PMCx_VLPS) if it has not been asserted previously.
- Go to the required low power mode (VLPR, LLS or VPLS).

The RBB regulators will be enabled in the mode transition.

Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1228)



Source: <https://www.nxp.com/docs/en/reference-manual/IMX7ULPRMB2.pdf> (Page 1150)

67. NXP has had knowledge of the '496 Patent at least as of the date when it was notified of the filing of this action.

68. Liberty Patents has been damaged as a result of the infringing conduct by NXP alleged above. Thus, NXP is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

69. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '496 Patent.

ADDITIONAL ALLEGATIONS REGARDING INFRINGEMENT AND PERSONAL JURISDICTION

70. NXP has also indirectly infringed the '504 Patent, the '156 Patent, and the '496 Patent by inducing others to directly infringe the '504 Patent, the '156 Patent, and the '496 Patent.

71. NXP has induced the end users and/or NXP's customers to directly infringe (literally and/or under the doctrine of equivalents) the '504 Patent, the '156 Patent, and the '496 Patent by using the accused products.

72. NXP took active steps, directly and/or through contractual relationships with others, with the specific intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, claim 9 of the '504 Patent, claim 9 of the '156 Patent, and claim 9 of the '496 Patent.

73. Such steps by NXP included, among other things, advising or directing customers and end users to use the accused products in an infringing manner; advertising and promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner.

74. NXP performed these steps, which constitute induced infringement, with the knowledge of the '504 Patent, the '156 Patent, and the '496 Patent and with the knowledge that the induced acts constitute infringement.

75. NXP was and is aware that the normal and customary use of the accused products by NXP's customers would infringe the '504 Patent, the '156 Patent, and the '496 Patent. NXP's inducement is ongoing.

76. NXP has also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to directly infringe (literally and/or under the doctrine of equivalents) the '504 Patent, the '156 Patent, and the '496 Patent by importing, selling or offering to sell the accused products.

77. NXP has a significant role in placing the accused products in the stream of commerce with the expectation and knowledge that they will be purchased by consumers in Texas and elsewhere in the United States.

78. NXP purposefully directs or controls the making of accused products and their shipment to the United States, using established distribution channels, for sale in Texas and elsewhere within the United States.

79. NXP purposefully directs or controls the sale of the accused products into established United States distribution channels, including sales to nationwide retailers. NXP's established United States distribution channels include one or more United States based affiliates.

80. NXP purposefully directs or controls the sale of the accused products online and in nationwide retailers, including for sale in Texas and elsewhere in the United States, and expects and intends that the accused products will be so sold.

81. NXP purposefully places the accused products—whether by itself or through subsidiaries, affiliates, or third parties—into an international supply chain, knowing that the accused products will be sold in the United States, including Texas. Therefore, NXP also facilitates the sale of the accused products in Texas.

82. NXP took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the '504 Patent, the '156 Patent, and the '496 Patent.

83. Such steps by NXP included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing

that such importation or sale would occur; and directing, facilitating, or influencing its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to import, sell, or offer to sell the accused products in an infringing manner.

84. NXP performed these steps, which constitute induced infringement, with the knowledge of the '504 Patent, the '156 Patent, and the '496 Patent, and with the knowledge that the induced acts would constitute infringement.

85. NXP performed such steps in order to profit from the eventual sale of the accused products in the United States.

86. NXP's inducement is ongoing.

87. NXP has also indirectly infringed by contributing to the infringement of the '504 Patent, the '156 Patent, and the '496 Patent. NXP has contributed to the direct infringement of the '504 Patent, the '156 Patent, and the '496 Patent by the end user of the accused products.

88. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the '504 Patent, the '156 Patent, and the '496 Patent, including, for example, claim 9 of the '504 Patent, claim 9 of the '156 Patent, and claim 9 of the '496 Patent.

89. The special features include, for example, components and/or features for applying body biasing voltages during a power mode of a processor or other integrated circuit in a manner that infringes the '504 Patent, the '156 Patent, and the '496 Patent.

90. These special features constitute a material part of the invention of one or more of the claims of the '504 Patent, the '156 Patent, and the '496 Patent, and are not staple articles of commerce suitable for substantial non-infringing use.

91. NXP's contributory infringement is ongoing.

92. NXP has had actual knowledge of the '504 Patent, the '156 Patent, and the '496 Patent at least as of the date when it was notified of the filing of this action. Since at least that time, NXP has known the scope of the claims of the '504 Patent, the '156 Patent, and the '496 Patent, the products that practice the '504 Patent, the '156 Patent, and the '496 Patent, and that Liberty Patents is the owner of the '504 Patent, the '156 Patent, and the '496 Patent.

93. By the time of trial, NXP will have known and intended (since receiving such notice) that its continued actions would infringe and actively induce and contribute to the infringement of one or more claims of the '504 Patent, the '156 Patent, and the '496 Patent.

94. Furthermore, NXP has a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of Liberty Patents' patent rights. *See, e.g.*, M. Lemley, "Ignoring Patents," 2008 Mich. St. L. Rev. 19 (2008).

95. NXP's actions are at least objectively reckless as to the risk of infringing valid patents, and this objective risk was either known or should have been known by NXP. NXP has knowledge of the '504 Patent, the '156 Patent, and the '496 Patent.

96. NXP's customers have infringed the '504 Patent, the '156 Patent, and the '496 Patent. NXP has encouraged its customers' infringement.

97. NXP's direct and indirect infringement of the '504 Patent, the '156 Patent, and the '496 Patent has been, and/or continues to be willful, intentional, deliberate, and/or in conscious disregard of Liberty Patents' rights under the patents-in-suit.

98. Liberty Patents has been damaged as a result of NXP's infringing conduct alleged above. Thus, NXP is liable to Liberty Patents in an amount that adequately compensates it for

such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Liberty Patents hereby requests a trial by jury on all issues so triable by right.

PRAYER FOR RELIEF

Liberty Patents requests that the Court find in its favor and against NXP, and that the Court grant Liberty Patents the following relief:

- a. Judgment that one or more claims of the '504 Patent, the '156 Patent, and the '496 Patent have been infringed, either literally and/or under the doctrine of equivalents, by NXP and/or all others acting in concert therewith;
- b. A permanent injunction enjoining NXP and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the '504 Patent, the '156 Patent, and the '496 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the '504 Patent, the '156 Patent, and the '496 Patent by such entities;
- c. Judgment that NXP account for and pay to Liberty Patents all damages to and costs incurred by Liberty Patents because of NXP's infringing activities and other conduct complained of herein, including an award of all increased damages to which Liberty Patents is entitled under 35 U.S.C. § 284;
- d. That Liberty Patents be granted pre-judgment and post-judgment interest on the damages caused by NXP's infringing activities and other conduct complained of herein;
- e. That this Court declare this an exceptional case and award Liberty Patents its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285; and
- f. That Liberty Patents be granted such other and further relief as the Court may

deem just and proper under the circumstances.

Dated: June 30, 2021

Respectfully submitted,

/s/ Zachariah S. Harrington

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